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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/747,965	Applicant(s) RADHAKRISHNAN ET AL.	
	Examiner John B. Vigushin	Art Unit 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004 & 28 Jun 2004*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-14* is/are allowed.

6)☒ Claim(s) *15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0705//11 Jul 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

2. Claims 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lockhart, Jr. (US 3,880,493).

As to Claim 15, Lockhart, Jr. discloses, in Figs. 1 and 2: a capacitor 37 with a plurality of openings 29; an IC (wafer) housed by an IC package 11 (col.1: 11-17); passing pins 15 from IC package 11 through openings 29 formed in capacitor 37; positioning capacitor 37 on a backside of IC package 11 directly underneath the IC; electrically connecting capacitor 37 to IC package 11 (col.3: 9-26).

As to Claim 16, Lockhart, Jr. further discloses electrically connecting IC package 11 to a socket 17 (which includes the capacitor 37; Fig. 2 and col.3: 9-10).

As to Claim 17, Lockhart, Jr. further discloses a plurality of first conductive layers 31; a plurality of second conductive layers 31 interleaved with the first conductive layers 31; and a plurality of dielectric layers separating adjacent conductive layers 31 (Fig. 2; col.3: 10-17).

As to Claim 18, Lockhart, Jr. further discloses, in Fig. 2, electrically coupling the first conductive layers 31 to a first node in the IC (through one of pins 15 located on--say, the left--side of the IC); and electrically coupling the second conductive layers to a

second node in the IC (through another of the pins 15 located on--say, the right--side of the IC).

Allowable Subject Matter

1. Claims 1-14 have been allowed over the prior art of record.

2. The following is an examiner's statement of reasons for allowance:

As to Claims 1-5, patentability resides in the combination of *first and second conductive vias **and** openings formed in the capacitor structure to enable pins from an integrated circuit package to pass through*, in combination with the other limitations of base Claim 1.

As to Claims 6-14, patentability resides in the combination of ***all*** elements of base Claim 6.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Devoe et al. (US 6,831,529) teaches the pins 16 carry an electronic signal (col.2: 34-37) and that the signal comes from a packaged electronic device (col.1: 17-

19), such as an implantable device (e.g., a pacemaker) but does not teach whether the device is a pin grid array (PGA) package and if so, whether or not pins 16 constitute the package pins of the PGA; and if the device is an IC package, Devoe et al. does not teach or fairly suggest that the capacitor 10 is located underneath the integrated circuit mounted on the PGA (or other type of connector) package.

b) Hernandez (Re. 35,064) discloses a capacitor with via holes for a dual in-line IC chip package (Figs. 10 and 11; col.6: 48-54) and does not teach an IC coupled to a first side of a package and the capacitor attached to a second side of the package.

c) Devey (US 2003/0147226 A1) discloses a BGA package 24 with an IC 10 coupled to a first side and a capacitor 46 attached to a second side underneath the IC 10 (Fig. 5; but does not teach that package 24 has pins and that the capacitor has openings for PGA package pins to pass through.

d) Naito et al. (US 6,678,145 B2) discloses a BGA package 63 with IC 64 coupled to a first side and a capacitor 41b attached to a second side underneath the IC 64 (Fig. 7) but does not teach that package 63 has pins and that the capacitor has openings for PGA package pins.

e) Herbert et al. (US 4,916,576) discloses a capacitor 98 with pins 116 for connecting to bus structures 130 and 132 (Fig. 12; col.8: 38-54).

f) Lockard et al. (US 4,626,958; already of record in Applicant's IDS of July 11, 2005) discloses, in Figs. 10A,B, a capacitor 60 with openings 63 in tabs 62 that receive the pins 66 of the PGA 64 but teaches that the capacitor 60 and the IC mounted to

package 64 (best seen in Fig. 3 and col.4: 21-23) are both on the same side of the package 64 (compare Figs. 3 and 10B).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
December 10, 2005